REMARKS

Reconsideration and reexamination of this application in light of the above-amendments and the following remarks is respectfully requested. Claims 1-15 and 20-29 are pending in this application. By way of this response, claims 24-29 have been amended and claim 30 has been added. Basis for the cosmetic changes made by way of this amendment can be found throughout the specification, claims, and drawings as originally filed. No new matter has been added. Reconsideration of the rejections set forth in the outstanding Office Action is respectfully requested in view of the preceding amended claims and the following remarks.

I. Allowable Subject Matter

Claims 10-15 have been allowed. Claims 21 and 23 stand objected to as being dependent upon a rejected based claim, but would be allowable if written in independent form including all of the limitations of the base claim and any intervening claims. Applicants greatly appreciate the indication of allowable subject matter.

II. Rejection Under 35 U.S.C. §102

Claims 1-9, 20, 22, and 24-29 stand rejected under 35 U.S.C. §102(e) as being anticipated by Quiet. In light of the above amendments and the following remarks, Applicants respectfully traverse the rejection.

Claims 1-9, and 20-23 are directed to a method and system for automatically generating a clock signal from one of a differential clock signal or a single-ended clock signal. The method includes determining whether the input clock signal is a differential clock signal or a single-ended clock signal. Based on the determination, an output clock signal is automatically generated.

Quiet discloses "a selectable input buffer circuit that receives external signals and processes the signals to output either a single-ended or a differential signal" (col. 3, lines 28-32). The selectable input buffer circuit selects between the single-ended and differential signal output (col. 3, lines 33-46). "If a differential signal is selected, the differential amplifier circuit generates a differential signal from the clock signal and the inverted clock signal." (col. 4, lines 53-57). "If a single-ended signal is selected, the inverted clock signal will be transmitted to the inverter circuit." (col. 4, lines 60-62). Quiet does not disclose determining whether an input clock signal is a differential clock signal or a single-ended clock signal.

Instead, Quiet is based on receiving two types of signals and then selecting the type of signal to be generated.

Claims 24-30 encompass a method and system that includes aligning an output single-ended clock signal with the received clock signal from which the output single-ended clock signal is derived.

Claims 25, 27 and 30 further include compensating for time delays associated with processing the received clock signal so that the output single-ended clock signal is aligned with the received clock signal.

Quiet does not disclose aligning an output clock signal with the received clock signal from which it is derived. Instead, Quiet discloses generating a selected type of signal. There is no attempt at aligning the generated signal with the input signals. In addition, Quiet does not disclose compensating for processing delays such as gate delays.

Thus as presently claimed, Applicants respectfully submit that claims 1-9 and 20-30 are not anticipated by Quiet. Accordingly, Applicants respectfully request reconsideration and withdrawal of this rejection of claims 1-9, 20, 22, and 24-29 under 35 U.S.C. §102(e).

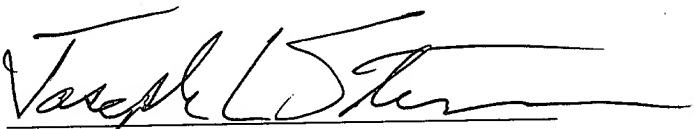
III. Conclusion

Applicants have carefully reviewed each of the objections and rejections set forth, and have amended the claims as indicated herein to individually address the rejections and objections and to place all claims in condition for allowance. In view of the above, Applicants submit that the specification and drawings are in order and that all the claims are now in condition for allowance. Such action is respectfully requested. Please apply any charges or credits to Deposit Account No. 06-1050. If the Examiner would like to discuss the matter further, the undersigned may be contacted at (858) 678-5070.

Attached is a marked-up version of the changes being made by the current amendment.

Respectfully submitted,

Date: October 3, 2002



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the claims:

Claims 16-19 have been cancelled.

Claim 30 has been added.

Claims 24-29 have been amended as follows:

24. (Amended) A method comprising:

receiving a clock signal, wherein the clock signal is one of a single-ended clock signal or a differential clock signal;

processing the clock signal wherein the processed clock signal has a time delay; [and]

generating an output single-ended clock signal that follows the received clock signal; and

aligning the output single-ended clock signal with the received clock signal.

25. (Amended) The method of claim 24 [further comprising aligning the output single-ended clock signal with the received clock signal] wherein aligning includes compensating for the processed clock signal time delay.

26. (Amended) A system comprising:

a clock generator, wherein the clock generator issues one of a single-ended clock signal or a differential clock signal; and

an electronic device including a first input terminal and a second input terminal, with the first input terminal coupled to the clock generator, [;

wherein] the electronic device [generates] to generate a single-ended clock signal of the same frequency as the clock signal issued by the clock generator and aligned with the clock signal issued by the clock generator.

27. (Amended) The system of claim 26, wherein the electronic device [issues a single-ended clock signal aligned with the clock signal issued by the clock generator] includes a phase lock loop to compensate for delays in processing the clock generator clock signal so that the electronic device single-ended clock signal is aligned with the clock generator clock signal.

28. (Amended) The system of claim 26,

[wherein the electronic device includes a first input terminal and a second input terminal, and]

wherein the electronic device couples the first input terminal [is coupled] to circuit ground when the clock generator issues a single-ended clock signal.

29. (Amended) The system of claim 26,

[wherein the electronic device includes a first input terminal and a second input terminal, and]

wherein the electronic device first and second input terminals are coupled to the clock generator when the clock generator issues a differential clock signal.